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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/469,406	12/22/99	KESHAVARZI A	042390.P7511

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EXAMINER	
KANG, D	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 11/08/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/469,406	KESHAVARZI ET AL.	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

in line 19 on page 5, the number "40" should be changed to "50".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claimed recitation does not supported by the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,4,8-14, 17, 21-22, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (Fig. 1 and Fig. 9) and Patwa (US 5,883,423).

Regarding claim **1**, admitted prior art by applicant (Fig. 1 and Fig. 9) discloses a die comprising (Fig. 1 and Fig. 9):

a first conductor carrying a power supply voltage (page 5, line 27); a second conductor carrying a ground voltage (page5, lines 28-29); and at least one semiconductor capacitor having a gate voltage (10 in Fig. 1).

Admitted prior art does not disclose the semiconductor capacitor operating in depletion mode between the first and second conductors to provide decoupling capacitance between the first and second conductor. However, when the power supply voltage (Vcc) of the capacitor 10 is between V_t and V_{FB}, the capacitor 10 has depletion mode to provide decoupling capacitance as shown in Fig. 3. See also page 6, line 23-26. This claim is operating of device rather than but product of semiconductor device.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to form decoupling capacitor in order to reduce the problem of noise arising due to parasitic inductance, resistance, and capacitance within integrated circuit.

Patwa et al discloses a die comprising (Fig. 2C):

a first conductor carrying a power supply voltage (202,204, and 214); a second conductor carrying a ground voltage (206); and at least one semiconductor capacitor (200) having a gate voltage (206).

Patwa does not disclose the semiconductor capacitor operating in depletion mode between the first and second conductors to provide decoupling capacitance between the first and second conductor.

However, this claim is operating of device rather than product of semiconductor device as discussed above. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to form decoupling capacitor in order to reduce the problem of noise arising due to parasitic inductance, resistance, and capacitance within integrated circuit.

Regarding claim **4**, admitted prior art discloses semiconductor capacitor in Fig. 1 having a P+ gate poly and P+ source/drain regions in an n-body. See page 5, lines 16-18.

Patwa et al discloses the at least one semiconductor capacitor having a P+ gate poly (206, Col.5, lines 42) and P+ source/drain regions (202 and 204) in an n-body (208).

Regarding claim **8**, prior art does not teach the power supply voltage has a smaller absolute value than does a flatband voltage. However, it is operation choice and would haven been obvious in the art at that time the invention was made to apply power supply voltage having less absolute value than a flatband voltage since any voltage can be applied to the capacitor.

Regarding claim **9**, admitted prior art discloses die further comprising (Fig. 9) voltage circuitry to provide a body voltage to the semiconductor capacitor and wherein the gate voltage is provided by the first conductor.

Regarding claim **10**, admitted prior art discloses a die further comprising (Fig.1) voltage circuitry to provide a body voltage to the at least one semiconductor capacitor and wherein the gate voltage is provided by the second conductor.

Patwa et al discloses a die further comprising voltage circuitry to provide a body voltage to the at least one semiconductor capacitor and wherein the gate voltage is provided by the second conductor (Col.5, lines 55-56).

Regarding claim **11**, admitted prior art discloses die further comprising (Fig. 1) voltage circuitry to provide the gate voltage and wherein a body voltage of the at least one semiconductor capacitor is provided by the first conductor.

Patwa et al discloses a die further comprising voltage circuitry to provide the gate voltage and wherein a body voltage of the at least one semiconductor capacitor is provided by the first conductor (Col.5, line 54).

Regarding claim **12**, admitted prior art discloses a die further comprising (Fig.9) voltage circuitry to provide the gate voltage and wherein a body voltage of the at least one semiconductor capacitor is provided by the second conductor.

Regarding claim **13**, admitted prior art does not discloses die further comprising additional capacitors between the first and second conductors at least some of which are not in the depletion mode.

However, it is well known and conventional to use in order to save cost of manufacturing.

Regarding claim **14**, admitted prior art (Fig. 1 and Fig. 9) discloses a die comprising:

a first conductor carrying a power supply voltage (page 5, lines 27-28); a second conductor carrying a ground voltage (page 5, lines 28029); and capacitors having: a conductive gate; an insulator dielectric and a semiconductor body.

Patwa et al also discloses a die comprising (Fig. 2C):

a first conductor carrying a power supply voltage (202,204, and 214); a second conductor carrying a ground voltage (206); and capacitors having: a conductive gate (206); an insulator dielectric (216) and a semiconductor body (208).

Both prior art does not teach the capacitor is in a depletion mode.

However, the capacitor 10 can have depletion mode if when the power supply voltage (Vcc) of the capacitor 10 is between V_t and V_{FB}. This claim is operating of device rather than product of semiconductor device as discussed above. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to form decoupling capacitor in order to reduce the problem of noise arising due to parasitic inductance, resistance, and capacitance within integrated circuit.

Regarding claim **17**, admitted prior art discloses semiconductor capacitor in Fig. 1 having a P+ gate poly and P+ source/drain regions in an n-body. See page 5, lines 16-18.

Patwa et al discloses the capacitor having a P+ gate poly (206, Col.5, lines 42) and P+ source/drain regions (202 and 204) in an n-body (208).

Regarding claim **21**, prior art does not teach the power supply voltage has a smaller absolute value than does a flatband voltage. However, it is operation choice and would haven been obvious in the art at that time the invention was made to apply power supply voltage having less absolute value than a flatband voltage since any voltage can be applied to the capacitor.

Regarding claim **22**, admitted prior art discloses a die comprising (Fig.1):

a first conductor carrying a power supply voltage (page 5, line 27); a second conductor conductor carrying a ground voltage (page5, lines 28-29); and at least one semiconductor capacitor (10) coupled between the first and second conductors to provide decoupling capacitance between the first and second conductors, the semiconductor capacitor having a gate voltage, the semiconductor capacitor having a flatband voltage (page 6, line 25) but does not teach the power supply voltage has a smaller absolute value than does the flatband voltage. However, it is well known as shown in Fig. 3 and conventional to have this voltage in order to obtain depletion mode. Therefore, It would have been obvious to one having ordinary skill in the art at the time the invention was made to apply this power voltage since it is required to have small voltage than flatband voltage to obtain depletion mode.

Regarding claim **25**, admitted prior art discloses semiconductor capacitor having a p+ gate poly and p+ source/drain regions in a p-body (Fig. 1).

4. Claims 2-3, 7, 15-16, 20,23-24, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (Fig. 9) in view of Chern et al (US 5,032,892).

Regarding claims **2**, **15**, and **23**, admitted prior art discloses all claimed invention except for semiconductor capacitor having an n-body. However, Chern et al teaches in Fig. 12C semiconductor capacitor having an n-body (113).

At the time the invention was made, it would have been an obvious matter of design choice to form n well claimed structure, since such a modification would have involved a mere change in the polarity type of a component.

Regarding claims **3, 16**, and **24**, admitted prior art (Fig. 9) as modified by Chern et al does not teach a poly gate having p+ type polarity. It would have been an obvious matter of design choice to form claimed structure, since such a modification would have involved a mere change in the polarity type of a component.

Regarding claim **7**, **20**, and **28**, admitted prior art (Fig. 1) does not teach semiconductor capacitor having a p-body. However, Chern et al discloses semiconductor capacitor having a p-body (Fig. 13).

5. Claims 5-6,18-19, and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (Fig. 1) in view of Chern et al (US 5,032,892).

Regarding claims **5**, **18**, and **26**, admitted prior art discloses a semiconductor capacitor having a p+ gate poly and p+ source/drain region but does not teach in a p-body. Chern et al teaches a semiconductor capacitor having a p-body. It would have been an obvious matter of design choice to form claimed structure, since such a modification would have involved a mere change in the polarity type of a component.

Regarding claims **6**, **19**, and **27**, admitted prior art (Fig. 1) as modified by Chern et al does not teach a poly gate having n+ type polarity. It would have been an obvious matter of design choice to form claimed structure, since such a modification would have involved a mere change in the polarity type of a component.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Donghee Kang** whose telephone number is 703-305-9147. The examiner can normally be reached on Monday – Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Donghee Kang

November 1, 2000

Steven Loke
Primary Examiner